Hardware Assisted Clock Synchronization for Real-Time Sensor Networks

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Utility of Clock Synchronization

Event Ordering

Predictable / Low duty-cycle Comm.
- TDMA
- Control Systems

Ranging / Localization
WSN Synchronization (1-3)

• Sensor Network Time Synchronization
  – Flooding Time Sync Protocol, FireFly-inspired Time Sync, Reference Broadcast, Glossy

• Larger Drift
• Fewer Samples
• Less Power

• Less Drift
• More Samples
• More Power
WSN Synchronization (2-3)

- Global Broadcasts
  - WWVB atomic clock, GPS, Radio Data Service (RDS)
  - Does not work well indoors
WSN Synchronization (3-3)

- Simultaneous Observations
  - Quasar Pulses, Quantum Entangled Particles
  - Not practical for low-power systems (yet)
Powerline Time Sync

Syntonistor

Mains  Powerline
Power line 60 Hz

• **Field Strength**
  - Home
    • 17 milli-gauss (as much as 10 gauss)
  - Industrial
    • As much as 100 gauss
  - Power Line
    • 3 milli-gauss at 60 meters
  - Earth
    • .02 milli-gauss

• **Stability**
  - $10^{-5}$ stability (typical oscillator is $10^{-5}$)
  - $10^{-8}$ differential delay stability between two points
  - Many old alarm clocks and appliances used the sine wave from direct contact to lines as a cheap clock
Wide Area Coverage
Phase Compensation Protocol

1. Build Spanning Tree
2. Flooding Time Synchronization
   - Determine phase offset from initial epoch
3. Phase Offset Adjustment
Syntonistor Benefits

• Once phase offsets have been established, the device remains synchronized for long periods of time \textit{without exchanging messages}.

• Errors can be detected by monitoring for rapid changes in the 60Hz signal.

• Stability of $10^{-5}$ (10μS/sec drift).

• \textit{Differential delay stability of $10^{-8}$} between two separated points (hundreds of miles).
Energy Accuracy Tradeoff

Can we do better?
Contributions Today

HW Clock Tuning Circuit

Improved Time Synchronization Hardware
Syntonistor v2
Syntonistor v2
Syntonistor v2

Antenna
Syntonistor v2

JFET Transistor
Syntonistor v2

Amplifier Stage 1
Syntonistor v2

Amplifier Stage 2
Syntonistor v2

Micro-controller running PLL
Improvements

Pros
+ more compact
+ lower-power
+ lower-cost
+ exhibit less jitter
+ noise immunity

Cons
- Sensitivity

Version 1

Version 2
Experimental Setup

Evaluate: Jitter, Sensitivity, Power (TBD)
Jitter Performance
Sensitivity

2 meters with a 10cm antenna
Clock Interfaces

Time Source (Syntonistor) → ? → Processor

Processor must wakeup to synchronize?
Hardware Clock Tuning

External Tuning Circuit
Hardware Clock Tuning

- DAC
- MSP430
- ATmega128RFA1
- 60Hz E-Field Front End
- X_IN
- X_OUT
- I2c
- PPS
- Error
- Sync
Hardware Clock Tuning

- Continuous Updates (tighter tracking)
- Updates while CPU sleeps
Stack
Pushing and Pulling the Clock

![Graph showing the relationship between DAC input and frequency delta (ppm).]
Impact of pushing and pulling

70°C Degree Swing
Power Performance

Total System Power: **17.44µW**
Rate Adjustment Frequency

Error due to change in drift rate

How can we reduce this error?

Clock Time

Real Time

Ideal Clock

Logical Clock

Hardware Unadjusted Clock

Clock Drift

Correction

Error

$t_0$, $t_1$, $t_2$, $t_3$, $t_4$, $t_5$
Rate Adjustment Frequency

- **Low adjustment period**
- **Ideal Clock**
- **High adjustment period**
- **Logical Clock**
- **Low adjustment period**
- **Logical Clock**
- **Hardware Unadjusted Clock**
- **Clock adjustment period reduced by factor of 3**
Error vs Rate Adjustment

- Adjustment period reduced by factor of 3
- Rate error reduced from 1.5 to 0.5
Energy Accuracy Tradeoff (revisited)
Limitations

Extra Hardware

System Time ≠ Wall Clock Time
Conclusions

• Improved Time Synchronization Circuit

• Low-cost HW clock rate adjustment

Improved EMF Clock + External HW Tuning = Power, Accuracy, Cost
Questions and comments?

THANKS!